Section 4. System Board I/O Controllers

Notes:

Keyboard/Auxiliary Device Controller

The keyboard/auxiliary device controller is a function of the Intel 8042 chip. The keyboard is connected to one of the two controller connectors in the rear of the system unit. This connector is dedicated to the keyboard. An auxiliary device connects to the other controller connector. The auxiliary device may be any type of serial input device compatible with the 8042 interface. Some of these are:

- Mouse
- Touchpad
- Trackball
- Keyboard.

The 8042 receives the serial data, checks the parity, translates keyboard scan codes (see bit 6 of the 8042 Command byte on page 4-9), and presents the data to the system as a byte of data at data port I/O address hex 0060. The interface can interrupt the system when data is available or can wait for polling from the microprocessor.

I/O address hex 0064 is the command/status port. When the system reads port hex 0064 it receives status information from the 8042. When the system writes to the port, the 8042 interprets the byte as a command.

The +5 Vdc line from the system board to the keyboard or auxiliary device has a fuse on the system board. The fuse status can be checked by issuing a Read Input Port command hex C0 to the keyboard controller. A 0 in bit position 3 of the input port indicates that the fuse is open.

Keyboard Password Security

The 8042 provides for a password security mechanism. Three commands are available regarding password operation:

A4	Test Password Installed
A5	Load Security
A6	Enable Security.

The system microprocessor may issue a Test Password Installed command to determine if a password is currently installed. This feature allows the controlling program to decide whether or not to write over the existing password.

The system microprocessor may issue a Load Security command and set a password in the 8042 at any time. Any existing password is lost, and the new password becomes the active password. The password must be installed in scan code format.

The system microprocessor must issue the Enable Security command to set the 8042 into secure mode. At this point the 8042 does not pass any information along to the system microprocessor. The 8042 intercepts the keyboard data stream, continuously comparing it to the installed password pattern. Until a match is encountered, all keyboard and auxiliary device data are not passed to the system microprocessor. When a match occurs the state of the 8042 is restored and data is allowed to pass to the system microprocessor.

The password may be changed as often as the system microprocessor chooses. No command to verify the installed password is provided. No commands are accepted by the 8042 when keyboard security is active.

8042 Command and Status Bytes

The following shows the 8042 Command and Status bytes:

Bit	Function
7	Reserved = 0
6	IBM Keyboard Translate Mode
5	Disable Auxiliary Device
4	Disable Keyboard
3	Reserved = 0
2	System Flag
1	Enable Auxiliary Interrupt
0	Enable Keyboard Interrupt

Figure 4-1. 8042 Command Byte, Port Hex 0064 Write

Bit 7 Reserved

Bit 6 When this bit is set to 1, the 8042 translates the incoming scan codes to scan code set 1 (used on the IBM Personal Computer and IBM Personal Computer XT). When set to 0 the 8042 passes the keyboard scan codes without translation.

Bit 5 Writing a 1 to this bit disables the auxiliary device interface by driving the 'clock' line low. Data is not sent or received.

Bit 4 Writing a 1 to this bit disables the keyboard interface by driving the 'clock' line low. Data is not sent or received.

Bit 3 Reserved

Bit 2 The value written to this bit is placed in the system flag bit of the 8042 Status register.

Bit 1 Writing a 1 to this bit causes the 8042 to generate an interrupt when it places auxiliary device data into its output buffer.

Bit 0 Writing a 1 to this bit causes the 8042 to generate an interrupt when it places keyboard data into its output buffer.

Bit	Function
7	Parity Error
6	General Time Out
5	Auxiliary Output Buffer Full
4	Inhibit Switch
3	Command/Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Figure 4-2. 8042 Status Byte, Port Hex 0064 Read

Input and Output Buffers

The output buffer is an 8-bit read-only register at I/O address hex 0060. When the output buffer is read, the 8042 uses it to send information to the system microprocessor. The information can be scan codes received from the keyboard, data from an auxiliary device, or data bytes that result from a command from the system microprocessor.

The input buffer is an 8-bit write-only register at I/O address hex 0060. When the input buffer is written, a flag is set that indicates a data write. Data written to I/O address hex 0060 is sent to the keyboard unless the 8042 is expecting a data byte following a 8042 command.

Data should be written to the 8042 input buffer only if the Input Buffer Full bit (bit 1) in the Status register (I/O address hex 0064) is equal to 0.

8042 Commands

A command is a data byte written to the 8042 through I/O address hex 0064. The following are the recognized commands, shown in hex values.

20-3F Read the 8042 RAM — Bits D5-D0 specify the address.

20 Read the 8042 Command Byte — The 8042 puts the command byte in its output buffer.

60-7F Write the 8042 RAM — Bits D5-D0 specify the address.

60 Write the 8042 Command Byte — The next byte of data written to I/O address hex 0060 is placed in the 8042 command byte. For more information on the 8042 Command byte see Figure 4-1 on page 4-9.

A4 Test Password Installed — This command checks if there is currently a password installed in the 8042. The test result is placed in the output buffer (I/O address hex 0060 and IRQ01). Hex FA means that the password is installed and hex F1 means that the password is not installed.

A5 Load Security — This command initiates the Password Load procedure. Following this command the 8042 will input from the data port until a null (0) is detected. The null terminates password entry.

A6 Enable Security — This command enables the 8042 security feature. This command is valid only when a password pattern is currently loaded into the 8042.

A7 Disable Auxiliary Device Interface — This command sets bit 5 of the 8042 command byte. This disables the auxiliary device interface by driving the 'clock' line low. Data is not sent or received.

A8 Enable Auxiliary Device Interface — This command clears bit 5 of the 8042 command byte, which releases the auxiliary device interface.

A9 Interface Test — This command causes the 8042 to test the auxiliary device clock and data lines. The test result is placed in the output buffer (I/O address hex 0060 and IRQ01) as shown in the following figure.

Test Result (hex)	Meaning
00	No Error Detected
01	The Auxiliary device 'Clock' line is stuck low.
02	The Auxiliary device 'Clock' line is stuck high.
03	The Auxiliary device 'Data' line is stuck low.
04	The Auxiliary device 'Data' line is stuck high.

Figure 4-3. Command A9 Test Results

AA Self Test — This command causes the 8042 to perform internal diagnostic tests. A hex 55 is placed in the output buffer if no errors are detected.

AB Interface Test – This command causes the 8042 to test the keyboard 'clock' and 'data' lines. The test result is placed in the output buffer (I/O address hex 0060 and IRQ01) as shown in the following figure.

Test Result (hex)	Meaning
00	No Error Detected
01	The keyboard 'Clock' line is stuck low.
02	The keyboard 'Clock' line is stuck high.
03	The keyboard 'Data' line is stuck low.
04	The keyboard 'Data' line is stuck high.

Figure 4-4. Command AB Test Results

AC Reserved

AD Disable Keyboard Interface – This command sets bit 4 of the 8042 Command byte. This disables the keyboard interface by driving the 'clock' line low. Data will not be sent or received.

AE Enable Keyboard Interface – This command clears bit 4 of the 8042 command byte, which releases the keyboard interface.

C0 Read Input Port – This command causes the 8042 to read its input port and place the data in its output buffer. This command should be used only if the output buffer is empty.

C1 Poll Input Port Low – Port 1 bits 0-3, in Status bits 4-7.

C2 Poll Input Port High – Port 1 bits 4-7, in Status bits 4-7.

D0 Read Output Port – This command causes the 8042 to read its output port and place the data in its output buffer. This command should be used only if the output buffer is empty.

D1 Write Output Port – The next byte of data written to I/O address hex 0060 is placed in the 8042 output port.

Note: Bit 0 of the 8042 output port is connected to System Reset. This bit should not be written low.

D2 Write Keyboard Output Buffer – The next byte written to I/O address hex 0060 input buffer is written to I/O address hex 0060 output buffer as if initiated by a device. An interrupt occurs if the interrupt is enabled in the Command byte.

D3 Write Auxiliary Device Output Buffer – The next byte written to I/O address hex 0060 input buffer is written to I/O address hex 0060 output buffer as if initiated by a device. An interrupt occurs if the interrupt is enabled in the Command byte.

D4 Write to Auxiliary Device – The next byte written to I/O address hex 0060 input buffer is transmitted to the auxiliary device.

E0 Read Test Inputs – This command causes the 8042 to read its T0 and T1 inputs. This data is placed in the output buffer. Data bit 0 represents T0 and data bit 1 represents T1.

F0-FF Pulse Output Port – Bits 0 through 3 of the 8042 output port may be pulsed low for approximately 6 microseconds. Bits 0 through 3 of this command indicate which bits are to be pulsed. A 0 indicates that the bit should be pulsed, a 1 indicates the bit should not be modified.

Note: Bit 0 of the 8042 output port is connected to System Reset. Pulsing of this bit resets the system microprocessor.

Keyboard/Auxiliary Device Programming Considerations

The following are some programming considerations for the Keyboard/Auxiliary device controller.

I/O address hex 0064 (Status register) can be read at any time.

I/O address hex 0060 should be read only when the Output Buffer Full bit in the Status register is a 1.

The Auxiliary Output Buffer Full bit in the Status register indicates that the data in I/O address hex 0060 came from the Auxiliary Device. This bit is valid only when the Output Buffer Full bit is a 1.

I/O address hex 0060 and I/O address hex 0064 should be written only when the Status register Input Buffer Full bit and the Output Buffer Full bit is 0.

The devices connected to the 8042 should be disabled before initiating a command that generates output. If output is generated, any value in the output buffer is overwritten.

An external latch is used to hold the level sensitive IRQ until an I/O read from address hex 0060 is executed by the system

Auxiliary Device/System Timings

Data transmissions to and from the auxiliary device connector consist of an 11-bit data stream sent serially over the 'data' line. The following figure shows the function of each bit.

Bit	Function
11	Stop bit (always 1)
10	Parity bit (odd parity)
9	Data bit 7 (most-significant)
8	Data bit 6
7	Data bit 5
6	Data bit 4
5	Data bit 3
4	Data bit 2
3	Data bit 1
2	Data bit 0 (least-significant)
1	Start bit (always 0)

Figure 4-5. Auxiliary Device Data Stream Bit Definitions

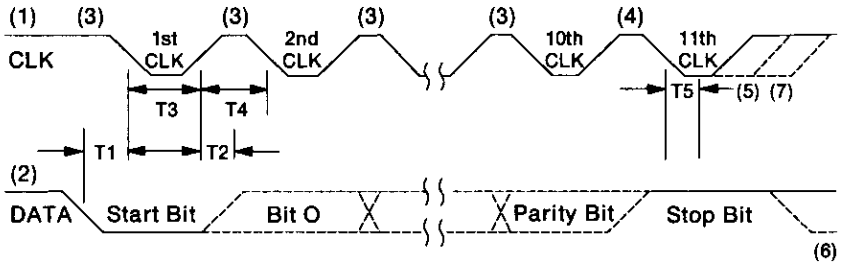
The parity bit is either 1 or 0, and the 8 data bits, plus the parity bit, always have an odd number of 1's.

System Receiving Data

The following describes the typical sequence of events that takes place when the system is receiving data from the auxiliary device. A graphic representation showing the timing relationships is presented in Figure 4-6 on page 4-15.

1. The auxiliary device checks the 'clock' line. If the line is inactive, output from the device is not allowed.
2. The auxiliary device checks the 'data' line. If the line is inactive, the device receives data from the system.

3. The auxiliary device checks the 'clock' line periodically during the transmission at intervals not exceeding 100 microseconds. If the device finds the system holding the 'clock' line inactive, the transmission is terminated. The system can terminate transmission anytime during the first ten clock cycles.
4. A final check for terminated transmission is performed at least 5 microseconds after the tenth clock.
5. The system can hold the 'clock' signal inactive to inhibit the next transmission.
6. The system can set the 'data' line inactive if it has a byte to transmit to the device. When the 'data' line is inactive, the system has data to transmit. The 'data' line is set inactive when the Start bit (always 0) is placed on the 'data' line.
7. The system raises the 'clock' line to allow the next transmission.



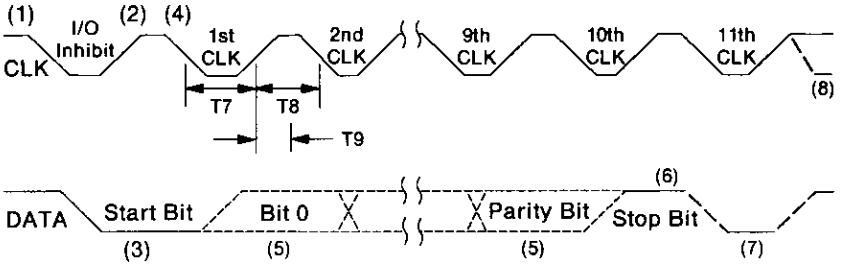
	Timing Parameter	Min/Max
T1	Time from DATA transition to falling edge of CLK	5 / 25 μsec
T2	Time from rising edge of CLK to DATA transition	5 / T4 - 5 μsec
T3	Duration of CLK inactive	30 / 50 μsec
T4	Duration of CLK active	30 / 50 μsec
T5	Time to auxiliary device inhibit after clock 11 to ensure the auxiliary device does not start another transmission	> 0 / 50 μsec

Figure 4-6. Receiving Data Timings

System Sending Data

The following describes the typical sequence of events that takes place when the system is sending data to the auxiliary device. A graphic representation showing the timing relationships is presented in Figure 4-7 on page 4-17.

1. The system checks for an auxiliary device transmission in process. If a transmission is in process and beyond the tenth clock, the system must receive the data.
2. The auxiliary device checks the 'clock' line. If the line is inactive, an I/O operation is not allowed.
3. The auxiliary device checks the 'data' line. If the line is inactive, the system has data to transmit. The 'data' line is set inactive when the Start bit (always 0) is placed on the 'data' line.
4. The auxiliary device sets the 'clock' line inactive. The system then places the first bit on the 'data' line. Each time the auxiliary device sets the 'clock' line inactive, the system places the next bit on the 'data' line until all bits are transmitted.
5. The auxiliary device samples the 'data' line for each bit while the 'clock' line is active. Data must be stable within 1 microsecond after the rising edge of the 'clock' line.
6. The auxiliary device checks for a positive level stop bit after the tenth clock. If the 'data' line is inactive, the auxiliary device continues to clock until the 'data' line becomes active, clocks the line-control bit, and at the next opportunity sends a Resend command to the system.
7. The auxiliary device pulls the 'data' line inactive, producing the line-control bit.
8. The system can pull the 'clock' line inactive, inhibiting the auxiliary device.



	Timing Parameter	Min/Max
T7	Duration of CLK inactive	30 / 50 μsec
T8	Duration of CLK active	30 / 50 μsec
T9	Time from inactive to active CLK transition, used to time when the auxiliary device samples DATA	5 / 25 μsec

Figure 4-7. Sending Data Timings

Signals

The keyboard and auxiliary device signals are driven by open-collector drivers pulled to 5 Vdc through 10 kilohm resistors. The following lists the characteristics of the signals.

Sink Current	20 mA	Maximum
High-level Output Voltage	5.0 Vdc minus pullup	Minimum
Low-level Output Voltage	0.5 Vdc	Maximum
High-level Input Voltage	2.0 Vdc	Minimum
Low-level Input Voltage	0.8 Vdc	Maximum

Figure 4-8. Keyboard/Auxiliary Device Signals

Connector

The keyboard and the auxiliary device connectors use 6-pin miniature DIN connectors. The signals and voltages are the same for both connectors. The following are the voltages and signals assigned to the keyboard and auxiliary device connectors.

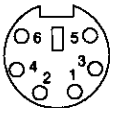


Figure 4-9. Keyboard and Auxiliary Device Connectors

Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 Vdc
5	I/O	Clock
6	NA	Reserved

Figure 4-10. Keyboard and Auxiliary Device Connectors Signal and Voltage Assignments