Diskette Drive Controller

The diskette drive controller and connector reside on the system board. In the Model 50 system, an interposer board plugs into the controller connector and provides connection for the diskette drives. In the Model 60 system a cable is used to connect the diskette drives to the system board.

Note: This section is included as a guide to compatibility for existing software. New software should access the diskette drive controller through BIOS.

The diskette drive controller supports:

- Two drives
- 1M byte unformatted media, 720K formatted
- 2M byte unformatted media, 1.44M formatted
- 250,000 bits-per-second mode
- 500,000 bits-per-second mode.

Precompensation of 125 nanoseconds is provided for all cylinders.

The diskette drive controller reads and writes both high- and low-density media. The 720K and 1.44M formatted diskette densities are supported for single and multithread operations.

Warning: 16-bit operations to the video subsystem can cause a diskette overrun in the 1.44M mode because data width conversions may require more than 12 microseconds. If an overrun occurs, BIOS returns an error code and the operation should be retried.

When switching from one density to another, the following changes occur:

- The clock rate changes.
  - Eight MHz for high density
  - Four MHz for low density
- The step rate changes.

Warning: The diskette controller does not check if the media supports the density selected. 1M media may not be reliably formatted to the 2M density and loss of data may result.

Registers

The diskette drive controller has five registers; three registers show the status of signals used in diskette operations, and two registers control certain interface signals. Two additional registers are accessed by the system microprocessor: the Diskette Drive Controller Status register and the Data register.

Status Register A: Status Register A, hex address 03F0, is a read-only register that shows the status of the corresponding signals.

Bit	Function
7	Interrupt Pending
6	-2nd Drive Installed
5	Step
4	-Track 0
3	Head 1 Select
2	-Index
1	-Write Protect
0	Direction

Figure 4-120. Status Register A (Hex 03F0)

Status Register B: Status Register B, address hex 03F1, is a read-only register that shows the status of signals between the diskette drive and the controller.

Bit	Function
7, 6	Reserved
5	Drive Select
4	Write Data (A positive transition on WR DATA causes this bit to toggle.)
3	Read Data (A positive transition on -RD DATA causes this bit to toggle.)
2	Write Enable
1	Motor Enable 1
0	Motor Enable 0

Figure 4-121. Status Register B (Hex 03F1)

Digital Output Register: The Digital Output register, address hex 03F2, is write-only and used to control drive motors, drive selection, and feature enable. All bits are cleared by a Reset.

Bit	Function
7, 6	Reserved
5	Motor Enable 1 *
4	Motor Enable 0 *
3	Reserved
2	-8272A Reset
1	Reserved
0	Drive Select (0 = Drive 0, 1 = Drive 1) *

* The Motor Enable bit is qualified by the Drive Select bit.

Figure 4-122. Digital Output Register (Hex 03F2)

Digital Input Register: The Digital Input register, address hex 03F7, is read-only and used to sense the state of the '-diskette change' signal and '-high density select' signal.

Bit	Function
7	Diskette Change
6 - 1	Reserved
0	-High Density Select

Figure 4-123. Digital Input Register (Hex 03F7)

Configuration Control Register: The Configuration Control register, address hex 03F7, is write-only and used to set the transfer rate.

Bit	Function
7 - 2	Reserved
1, 0	DRC1, DRC0 00 = 500,000-bit mode 01 = Reserved 10 = 250,000-bit mode 11 = Reserved

Figure 4-124. Configuration Register (Hex 03F7)

Diskette Drive Controller Status Register: This is a read-only register and is used to facilitate the transfer of data between the system microprocessor and the controller.

Bit	Function
7	Request for Master
6	Data Input/Output
5	Non-DMA Mode
4	Diskette Controller Busy
3	Reserved
2	Reserved
1	Drive 1 Busy
0	Drive 0 Busy

Figure 4-125. Diskette Drive Controller Status Register (Hex 03F4)

Bit 7 When this bit is set to 1, the Data register is ready for transfer with the system microprocessor.

Bit 6 This bit indicates the direction of data transfer between the diskette drive controller and the system microprocessor. If this bit is set to 1, the transfer is from the controller to the system microprocessor; if it is set to 0, the transfer is from the microprocessor.

Bit 5 When this bit is set to 1, the controller is in the non-DMA mode.

Bit 4 When this bit is set to 1, a Read or Write command is being executed.

Bit 3, 2 Reserved

Bit 1 Drive 1 Busy - When set to 1, diskette drive 1 is in the seek mode.

Bit 0 Drive 0 Busy - When set to 1, diskette drive 0 is in the seek mode.

Data Registers, Hex 03F5: Address hex 03F5, consists of several registers in a stack with only one register presented to the data bus at a time. It stores data, commands, and parameters, and provides diskette-drive status information. Data bytes are passed through the Data register to program or obtain results after a command.

Diskette Drive Controller Programming Considerations

Each command is initiated by a multibyte transfer from the system microprocessor, and the result can also be a multibyte transfer back to the system microprocessor. Because of this multibyte interchange of information between the controller and the microprocessor, each command is considered to consist of three phases:

Command Phase: The system microprocessor issues a series of Writes to the controller that direct it to perform a specific operation.

Execution Phase: The controller performs the specified operation.

Result Phase: After completion of the operation, status and other housekeeping information is made available to the system microprocessor through a sequence of Read commands to the system microprocessor.

The following is a summary of the commands that are issued to the diskette drive controller.

- Read Data command
- Read Deleted Data command
- Read a Track command
- Read ID command
- Write Data command
- Write Deleted Data command
- Format a Track command
- Scan Equal command
- Scan Low or Equal command
- Scan High or Equal command
- Recalibrate command
- Sense Interrupt Status command
- Specify command
- Sense Drive Status command
- Seek command.

The following figure shows the symbols used in the format of the individual commands. The individual command formats start on page 4-133.

Symbol	Name	Description
C	Cylinder Number	C contains the current or selected cylinder number in binary notation.
D	Data	D contains the data pattern to be written to a sector.
D7-D0	Data Bus	An 8-bit data bus in which D7 is the most-significant bit and D0 is the least significant.
DTL	Data Length	When N is 00, DTL is the data length to be read from or written to a sector.
EOT	End of Track	The final sector number on a cylinder.
GPL	Gap Length	The length of gap 3 (spacing between sectors excluding the voltage controlled oscillator synchronous field).
H	Head Address	The head number, either 0 or 1, as specified in the ID field.
HD	Head	The selected head number, 0 or 1. (H=HD in all command words.)
HLT	Head Load Time	The head load time in the selected drive (2 to 254 milliseconds in 2-millisecond increments).
HUT	Head Unload Time	The head unload time after a Read or Write operation (16 to 240 milliseconds in 16-millisecond increments).
MF	FM or MFM Mode	A 0 selects FM mode and a 1 selects MFM.
MT	Multitrack	A 1 selects multitrack operation. (Both HD0 and HD1 will be read or written.)

Figure 4-126 (Part 1 of 2). Command Symbols, Diskette Drive Controller

Symbol	Name	Description
N	Number	The number of data bytes written in a sector.
NCN	New Cylinder Number	The new cylinder number for a seek operation.
ND	Non-DMA Mode	This indicates an operation in the non-DMA mode.
PCN	Present Cylinder Number	The cylinder number at the completion of a Sense Interrupt Status command (present position of the head).
R	Record	The sector number to be read or written.
SC	Sector	The number of sectors per cylinder.
SK	Skip	This stands for skip deleted-data address mark.
SRT	Step Rate	The stepping rate for the diskette drive (1 to 16 milliseconds in 1-millisecond increments).
ST 0 - ST 3	Status 0-Status 3	Four registers that store status information after a command is executed.
STP	Scan Test	If STP is 1, the data in contiguous sectors is compared with the data sent by the system microprocessor during a scan operation. If STP is 2, then alternate sectors are read and compared.
US0 - US1	Unit Select	The selected drive number encoded the same as bits 0 and 1 of the Digital Output register.

Figure 4-126 (Part 2 of 2). Command Symbols, Diskette Drive Controller

The following are commands that are issued to the controller. An X is used to indicate a don't care condition.

Read Data Command Format

Command Phase

MT = Multitrack
MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	0	1	1	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Data Length (DTL) Bits 7 - 0							

Figure 4-127. Read Data Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-128. Read Data Result

Read Deleted Data Command Format

Command Phase

MT = Multitrack
MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	0	1	1	0	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Data Length (DTL) Bits 7 - 0							

Figure 4-129. Read Deleted Data Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-130. Read Deleted Data Result

Read a Track Command Format

Command Phase

MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	0	MF	SK	0	0	0	1	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Data Length (DTL) Bits 7 - 0							

Figure 4-131. Read a Track Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-132. Read a Track Result

Read ID Command Format

Command Phase

MF = MFM mode
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	0	1	0
Byte 1	X	X	X	X	X	HD	US1	US0

Figure 4-133. Read ID Command

Result Phase

	7 6 5 4 3 2 1 0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0
Byte 1	Status Register 1 (ST 1) Bits 7 - 0
Byte 2	Status Register 2 (ST 2) Bits 7 - 0
Byte 3	Cylinder Number (C) Bits 7 - 0
Byte 4	Head Address (H) Bits 7 - 0
Byte 5	Sector Number (R) Bits 7 - 0
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0

Figure 4-134. Read ID Result

Write Data Command Format

Command Phase

MT = Multitrack
MF = MFM mode
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	0	1	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Data Length (DTL) Bits 7 - 0							

Figure 4-135. Write Data Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-136. Write Data Result

Write Deleted Data Command Format

Command Phase

MT = Multitrack
MF = MFM mode
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	0	0	1	0	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Data Length (DTL) Bits 7 - 0							

Figure 4-137. Write Deleted Data Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-138. Write Deleted Data Result

Format a Track Command Format

Command Phase

MF = MFM mode
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	0	MF	0	0	1	1	0	0
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 3	Sectors per Cylinder (SC) Bits 7 - 0							
Byte 4	Gap Length (GPL) Bits 7 - 0							
Byte 5	Data (D) Bits 7 - 0							

Figure 4-139. Format a Track Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of data bytes in sector (N) Bits 7 - 0							

Figure 4-140. Format a Track Result

Scan Equal Command Format

Command Phase

MT = Multitrack
MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	0	0	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Scan Test (STP) Bits 7 - 0							

Figure 4-141. Scan Equal Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-142. Scan Equal Result

Scan Low or Equal Command Format

Command Phase

MT = Multitrack
MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	1	0	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Scan Test (STP) Bits 7 - 0							

Figure 4-143. Scan Low or Equal Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-144. Scan Low or Equal Result

Scan High or Equal Command Format

Command Phase

MT = Multitrack
MF = MFM mode
SK = Skip deleted-data address mark
HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	MT	MF	SK	1	1	1	0	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	Cylinder Number (C) Bits 7 - 0							
Byte 3	Head Address (H) Bits 7 - 0							
Byte 4	Sector Number (R) Bits 7 - 0							
Byte 5	Number of Data Bytes in Sector (N) Bits 7 - 0							
Byte 6	End of Track (EOT) Bits 7 - 0							
Byte 7	Gap Length (GPL) Bits 7 - 0							
Byte 8	Scan Test (STP) Bits 7 - 0							

Figure 4-145. Scan High or Equal Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 0 (ST 0) Bits 7 - 0							
Byte 1	Status Register 1 (ST 1) Bits 7 - 0							
Byte 2	Status Register 2 (ST 2) Bits 7 - 0							
Byte 3	Cylinder Number (C) Bits 7 - 0							
Byte 4	Head Address (H) Bits 7 - 0							
Byte 5	Sector Number (R) Bits 7 - 0							
Byte 6	Number of Data Bytes in Sector (N) Bits 7 - 0							

Figure 4-146. Scan High or Equal Result

Recalibrate Command Format

Command Phase

USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	1	1
Byte 1	X	X	X	X	X	0	US1	US0

Figure 4-147. Recalibrate Command

Result Phase: This command has no result phase.

Sense Interrupt Status Command Format

Command Phase

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	0	0	0

Figure 4-148. Sense Interrupt Status Command

Result Phase

	7 6 5 4 3 2 1 0
Byte 0	Status Register 0 (ST 0)
Byte 1	Present Cylinder Number (PCN)

Figure 4-149. Sense Interrupt Status Result

Specify Command Format

Command Phase

SRT = Diskette stepping rate
HUT = Head unload time
HLT = Head load time
ND = Non-data mode

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	0	1	1
Byte 1	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT
Byte 2	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND

Figure 4-150. Specify Command

Result Phase: This command has no result phase.

Sense Drive Status Command Format

Command Phase

HD = Head number
USx = Unit select

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	1	0	0
Byte 1	X	X	X	X	X	HD	US1	US0

Figure 4-151. Sense Drive Status Command

Result Phase

	7	6	5	4	3	2	1	0
Byte 0	Status Register 3 (ST 3) Bits 7 - 0							

Figure 4-152. Sense Drive Status Result

Seek Command Format

Command Phase

USx = Unit select
HD = Head select

	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	1	1	1	1
Byte 1	X	X	X	X	X	HD	US1	US0
Byte 2	New Cylinder Number for Seek (NCN) Bits 7 - 0							

Figure 4-153. Seek Command

Result Phase: This command has no result phase.

Invalid Command Format

Result Phase: The following status byte is returned to the system microprocessor when an invalid command has been received.

	7	6	5	4	3	2	1	0
Byte 0	Status 0 Register (ST 0) Bits 7 - 0							

Figure 4-154. Invalid Command Result

Command Status Registers

The following are definitions of status registers ST 0 through ST 3.

Status Register 0: The following are bit definitions of status register ST 0.

Bit	Function
7, 6	Interrupt Code (IC) 00 = Normal Termination of Command (NT) - The command was completed and properly executed. 01 = Abrupt Termination of Command (AT) - The execution of the command was started but not successfully completed. 10 = Invalid Command Issue (IC) - The issued command was never started. 11 = Reserved
5	Seek End (SE) - Set to 1 when the diskette drive completes the Seek command.
4	Equipment Check (EC) - Set to 1 if the '-track 0' signal fails to occur after 77 step pulses (Recalibrate command).
3	Not Ready (NR) - This flag is set to 1 when the diskette drive is in the not-ready state and a Read or Write command is issued. It is also set if a Read or Write command is issued to side 1 of a single-sided diskette drive.
2	Head Address (HD) - Indicates the state of the head at interrupt.
1	Unit select 1 (US 1) - Indicates drive 1 is at interrupt.
0	Unit select 0 (US 0) - Indicates drive 0 is at interrupt.

Figure 4-155. Status Register 0 (ST 0)

Status Register 1: The following are bit definitions of status register ST 1.

Bit	Function
7	End of Cylinder (EN) - Set to 1 when the controller tries to gain access to a sector beyond the final sector of a cylinder.
6	Reserved - This bit is always set to 0.
5	Data Error (DE) - Set to 1 when the controller detects a CRC error in either the ID field or the data field.
4	Overrun (OR) - Set to 1 if the controller is not serviced by the main system within a certain time limit during data transfers.
3	Reserved - This bit is always set to 0.
2	No Data (ND) - Set to 1 if the controller cannot find the sector specified in the ID register during the execution of a Read Data, Write Deleted Data, or Scan command. This flag is also set to 1 if the controller cannot read the ID field without an error during the execution of a Read ID command or if the starting sector cannot be found during the execution of a Read Cylinder command.
1	Not Writable (NW) - Set to 1 if the controller detects a '-write-protect' signal from the diskette drive during execution of a Write Data, Write Deleted Data, or Format Cylinder command.
0	Missing Address Mark (MA) - Set to 1 if the controller cannot detect the ID address mark. At the same time, the MD of Status register 2 is set to 1.

Figure 4-156. Status Register 1 (ST 1)

Status Register 2: The following are bit definitions of status register ST 2.

Bit	Function
7	Reserved - This bit is always set to 0.
6	Control Mark (CM) - This flag is set to 1 if the controller encounters a sector that has a deleted data-address mark during execution of a Read Data or Scan command.
5	Data Error in Data Field (DD) - Set to 1 if the controller detects an error in the data.
4	Wrong Cylinder (WC) - This flag is related to ND (no data) bit. When the contents of C on the medium are different from that stored in the ID register, this flag is set.
3	Scan Equal Hit (SH) - Set to 1 if the contiguous sector data equals the processor data during the execution of a Scan command.
2	Scan Not Satisfied (SN) - Set to 1 if the controller cannot find a sector on the cylinder that meets the condition during a Scan command.
1	Bad Cylinder (BC) - Related to ND; when the contents of C on the medium are different from that stored in the ID register, and the contents of C is FF, this flag is set to 1.
0	Missing Address Mark in Data Field (MD) - Set to 1 if the controller cannot find a data address mark or a deleted data address mark when data is read from the medium.

Figure 4-157. Status Register 2 (ST 2)

Status Register 3: The following are bit definitions of status register ST 3.

Bit	Function
7	Reserved
6	Write Protect (WP) - Status of the '-write-protect' signal from the diskette drive.
5	Reserved
4	Track 0 (T0) - Status of the '-track 0' signal from the diskette drive.
3	Reserved
2	Head Address (HD) - Status of the '-head 1 select' signal to the diskette drive.
1, 0	Reserved

Figure 4-158. Status Register 3 (ST 3)

Signal Descriptions

The diskette drive controller interface signal sequences and timings are all compatible with the industry standard 5.25 inch diskette interface. All interface signals are TTL compatible at the driver/receivers both in the rise and fall times as well as the interface levels.

The following describes the interface to the diskette drive.

Output Signals

All output signals to the diskette drive operate between 5 Vdc and ground with the following definitions:

- The inactive level is 2.0 Vdc minimum.
- The active level is 0.8 Vdc maximum.

All inputs from the drive can sink 4.0 mA at the active (low) level.

- The inactive level is 3.7 Vdc minimum.
- The active level is 0.4 Vdc maximum.

The following are descriptions of the diskette drive controller output signals.

-HIGH DENSITY SELECT: When active, the 2M mode is selected. Diskettes will be formatted with 18 sectors per track and a capacity of 1.44M. When inactive, the 1M mode is selected. Diskettes will be formatted with 9 sectors per track and a capacity of 720K. This signal is not used by the 720K diskette drive.

-DRIVE SELECT 0 - 1: The drive select signals enable or disable all drive interface signals except -MOTOR ENABLE. When a drive select signal is active, the drive is enabled. When it is inactive, all controlled inputs are ignored, and all drive outputs are disabled.

-MOTOR ENABLE 0 - 1: When this signal is made active, along with the proper drive select signals, the spindle starts to turn. There must be a 500-millisecond delay after -MOTOR ENABLE 0 or -MOTOR ENABLE 1 becomes active before a read, write, or seek operation. When inactive, this signal causes the spindle motor to decelerate and stop.

-DIRECTION: When this signal is active, -STEP moves the heads toward the drive spindle. When this signal is inactive, -STEP moves the heads away from the drive spindle. This signal is stable for 1 microsecond before and 1 microsecond after the trailing edge of the step pulse.

Note: After a direction change, a 15-millisecond delay is required before the next '-step' pulse.

-STEP: A 1-microsecond active pulse of this signal causes the read/write heads to move one track. The state of -DIRECTION at the trailing edge of -STEP determines the direction of motion.

Note: Before a read or write operation, a 15-millisecond seek settle time must be allowed.

-WRITE DATA: A 250-nanosecond pulse of this signal causes a bit to be written if -WRITE ENABLE is active. Data written on the diskette will have 125-nanosecond write-precompensation.

-WRITE ENABLE: When active, this signal enables the write current circuits, and -WRITE DATA controls the writing of information. Motor-start and head-settle times must be observed before this line becomes active.

-HEAD 1 SELECT: Making this signal active selects the upper head; otherwise the lower head is selected.

Input Signals

All inputs from the drive can sink 4.0 mA at the active (low) level.

- The inactive level is 3.7 Vdc minimum.
- The active level is 0.4 Vdc maximum.

-INDEX: When the drive senses the index, it generates an active pulse of at least 1 millisecond on this line. This signal is gated to the interface only when a diskette is in the drive.

-TRACK 0: This signal is active when the read/write head is on track 0. Track 0 is determined by a sensor, not a track counter.

The drive is able to seek to track 0 under control of the system even if there is no diskette inserted at the time. This is required so the system software can determine how many drives are attached to the system. Software selects each drive and attempts to recalibrate that drive to track 0. The track 0 indication is used to determine whether or not each drive is installed in the system.

-WRITE PROTECT: When active, this signal indicates that a diskette with an open write-protect window (write-protected diskette) is in the drive, and the drive will not write.

-READ DATA: Each bit detected provides a 250-nanosecond active pulse on this line for the 250,000 bit rate or a 125-nanosecond pulse for the 500,000 bit rate.

-DISKETTE CHANGE: This signal is active at power-on and latched inactive when a diskette is present, the drive is selected, and a step pulse occurs. This signal goes active when the diskette is removed from the drive. The presence of a diskette is determined by a media sensor.

Power Sequencing

The WRITE GATE signal is turned off and is kept off before power is switched on or off. The read/write heads return to track 0 when the system power is switched on.

Connector

The diskette drives for the Model 50 attach to the system board through an interposer board. The Model 60 diskette drives attach to the system board through a cable.

The diskette drive connector on the Model 50 system board is a 50-pin printed circuit board edge connector.

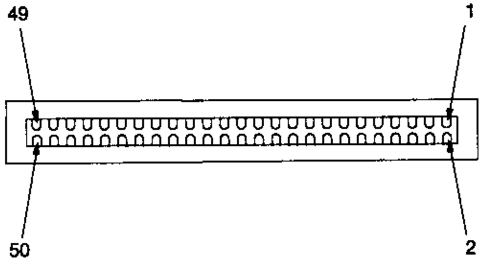

Figure 4-159. Model 50 Diskette Drive Controller Connector

The following are the voltages and signals assigned to the diskette drive controller connector.

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I	2nd Drive Installed	2	O	-High Density Select
3	NA	Ground	4	NA	Ground
5	NA	Ground	6	NA	Reserved
7	NA	Signal Ground	8	I	-Index
9	NA	Signal Ground	10	O	-Motor Enable 0
11	NA	Signal Ground	12	O	-Drive Select 1
13	NA	Ground	14	O	-Drive Select 0
15	NA	Signal Ground	16	O	-Motor Enable 1
17	NA	Signal Ground	18	O	-Direction
19	NA	Signal Ground	20	O	-Step
21	NA	Signal Ground	22	O	-Write Data
23	NA	Signal Ground	24	O	-Write Enable
25	NA	Signal Ground	26	I	-Track 0
27	NA	Signal Ground	28	I	-Write Protect
29	NA	Signal Ground	30	I	-Read Data
31	NA	Signal Ground	32	O	-Head 1 Select
33	NA	Signal Ground	34	I	-Diskette Change
35	NA	Ground	36	NA	Ground
37	NA	Ground	38	NA	+5 Vdc
39	NA	Ground	40	NA	+12 Vdc
41	NA	Reserved	42	NA	Reserved
43	NA	Reserved	44	NA	Reserved
45	NA	Reserved	46	NA	Reserved
47	NA	Reserved	48	NA	Reserved
49	NA	Reserved	50	NA	Reserved

Figure 4-160. Model 50 Diskette Drive and Interposer Board Connector Voltage and Signal Assignments

The Model 60 system board has a single 2-by-20 pin connector for the attachment of one or two diskette drives. Signals and data are transmitted to and from the drives through a 40-wire L-shaped cable.

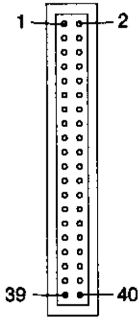

Figure 4-161. Model 60 Diskette Drive Controller Connector

The following are the voltages and signals assigned to the diskette drive controller connector.

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I	2nd Drive Installed	2	O	-High Density Select
3	NA	Ground	4	NA	Ground
5	NA	Ground	6	NA	Reserved
7	NA	Signal Ground	8	I	-Index
9	NA	Signal Ground	10	O	-Motor Enable 0
11	NA	Signal Ground	12	O	-Drive Select 1
13	NA	Ground	14	O	-Drive Select 0
15	NA	Signal Ground	16	O	-Motor Enable 1
17	NA	Signal Ground	18	O	-Direction
19	NA	Signal Ground	20	O	-Step
21	NA	Signal Ground	22	O	-Write Data
23	NA	Signal Ground	24	O	-Write Enable
25	NA	Signal Ground	26	I	-Track 0
27	NA	Signal Ground	28	I	-Write Protect
29	NA	Signal Ground	30	I	-Read Data
31	NA	Signal Ground	32	O	-Head 1 Select
33	NA	Signal Ground	34	I	-Diskette Change
35	NA	Ground	36	NA	Ground
37	NA	Ground	38	NA	+ 5 Vdc
39	NA	Ground	40	NA	+ 12 Vdc

Figure 4-162. Model 60 Diskette Drive Controller Connector Voltage and Signal Assignments

Serial Port Controller

The serial port is controlled by a NS16550 serial communications controller. It is programmable and supports asynchronous communications. The controller automatically adds and removes start, stop, and parity bits. A programmable baud-rate generator allows operation from 50 baud to 19,200 baud. The port supports 5-, 6-, 7- and 8-bit characters with 1, 1.5, or 2 stop bits. A prioritized interrupt system controls transmit, receive, error, and line status as well as data-set interrupts.

The NS16550 controller is functionally compatible to the NS16450 controller. To programs, the NS16550 appears to be identical to the serial portion of the IBM Personal Computer AT Serial/Parallel adapter. Support for the controller is restricted to the functions which are identical to the NS16450. Using the controller in the FIFO mode may result in non-detectable data errors.

The serial port controller provides the following functions:

- Full double buffering in the character mode, eliminating the need for precise synchronization
- False-start bit detection
- Line-break generation and detection
- Modem control functions:
  - Clear to send (CTS)
  - Request to send (RTS)
  - Data set ready (DSR)
  - Data terminal ready (DTR)
  - Ring indicator (RI)
  - Data carrier detect (DCD).

The following figure is a block diagram of the serial port controller.

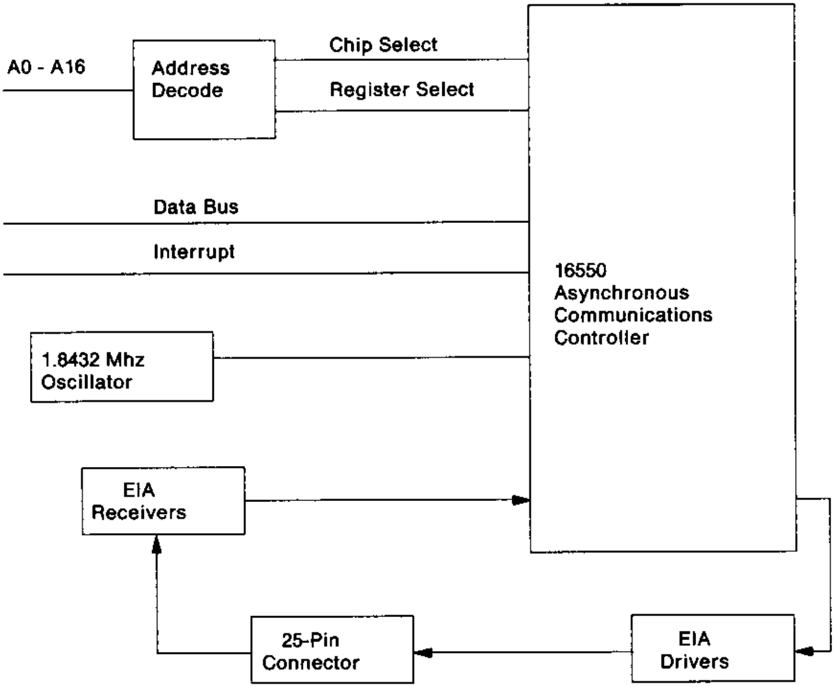

Figure 4-163. Serial Port Block Diagram

Communications Application

The serial output port can be addressed as either serial output port 1 (Serial 1) or serial output port 2 (Serial 2). In this section port addresses contain an **n**. The **n** can be either a 3 for Serial 1 or a 2 for Serial 2. The selection of either port is discussed in "System Board Setup" on page 2-24.

Two interrupt lines are provided to the system. Interrupt level 4 (IRQ4) is for Serial 1 and interrupt level 3 (IRQ3) is for Serial 2. To allow the controller to send interrupts to the interrupt controller, bit 3 of the Modem Control register must be set to 1. At this point, any interrupts allowed by the Interrupt Enable register will cause an interrupt.

The data format is as follows:

Marking	Start Bit	D0	D1	D2	D3	D4	D5	D6	D7	Parity Bit	Stop Bit

Figure 4-164. Serial Port, Data Format

Data bit 0 is the first bit to be sent or received. The controller automatically inserts the start bit, the correct parity bit (if programmed to do so), and the stop bits (1, 1.5, or 2, depending on the command in the Line Control register).

Programmable Baud-Rate Generator

The controller has a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 65,535. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during setup to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

Registers

The controller has a number of accessible registers. The system programmer may gain access to or control any of the controller registers through the system microprocessor. These registers are used to control the controller operations and to transmit and receive data.

Specific registers are selected according to the following figure:

DLAB State *	Port Address (hex)	R/W	Register
0	0nF8 **	W	Transmitter Holding Register **n**
0	0nF8 **	R	Receiver Buffer Register **n**
1	0nF8 **	R/W	Divisor Latch, Low Byte
1	0nF9 **	R/W	Divisor Latch, High Byte
0	0nF9 **	R/W	Interrupt Enable Register
X	0nFA **	R	Interrupt Identification Register
X	0nFA **	W	FIFO Control Register
X	0nFB **	R/W	Line Control Register
X	0nFC **	R/W	Modem Control Register
X	0nFD **	R	Line Status Register
X	0nFE **	R	Modem Status Register
X	0nFF **	R/W	Scratch Register

* The DLAB state is controlled by bit 7 of the Line Control register.
** The **n** determines the port selected; 3 is for Serial 1, and 2 is for Serial 2.

Figure 4-165. Serial Port Register Addresses

Transmitter Holding Register (hex nF8)

The Transmitter Holding register contains the character to be sent. Bit 0 is the least-significant bit and the first bit sent serially as shown in the following figure:

Bit	Function
7	Data Bit 7
6	Data Bit 6
5	Data Bit 5
4	Data Bit 4
3	Data Bit 3
2	Data Bit 2
1	Data Bit 1
0	Data Bit 0

Figure 4-166. Transmitter Holding Register (THR)

Receiver Buffer Register (hex nF8)

The Receiver Buffer register (RBR) contains the received character. Bit 0 is the least-significant bit and the first bit received serially as shown in the following figure:

Bit	Function
7	Data Bit 7
6	Data Bit 6
5	Data Bit 5
4	Data Bit 4
3	Data Bit 3
2	Data Bit 2
1	Data Bit 1
0	Data Bit 0

Figure 4-167. Receiver Buffer Register (RBR)

Divisor Latch Register LSB (hex nF8)

Bit	Function
7	Bit 7
6	Bit 6
5	Bit 5
4	Bit 4
3	Bit 3
2	Bit 2
1	Bit 1
0	Bit 0

Figure 4-168. Divisor Latch Register (LSB)

Divisor Latch Register MSB (hex nF9)

Bit	Function
7	Bit 7
6	Bit 6
5	Bit 5
4	Bit 4
3	Bit 3
2	Bit 2
1	Bit 1
0	Bit 0

Figure 4-169. Divisor Latch Register (MSB)

The Divisor Latch registers are used to program the baud rate generator. The values in these two registers form the divisor of the clock input (1.8432 MHz), which establishes the desired baud rate.

The following figure illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 19,200 and below, the error obtained is minimal.

Note: In no case should the data speed be greater than 19,200 baud.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent of Error Difference Between Desired and Actual
50	2304	0900	--
75	1536	0600	--
110	1047	0417	0.026
134.5	857	0359	0.058
150	768	0300	--
300	384	0180	--
600	192	00C0	--
1200	96	0060	--
1800	64	0040	--
2000	58	003A	0.69
2400	48	0030	--
3600	32	0020	--
4800	24	0018	--
7200	16	0010	--
9600	12	000C	--
19200	6	0006	--

Figure 4-170. Baud Rates at 1.8432 MHz

Interrupt Enable Register (hex nF9)

This 8-bit register allows the four types of controller interrupts to separately activate the 'chip-interrupt' output signal. The interrupt system can be totally disabled by clearing bits 0 through 3 of the Interrupt Enable register. Similarly, by setting the appropriate bits of this register to 1, selected interrupts can be enabled. Disabling the interrupts inhibits the 'chip-interrupt' output signal from the controller. All other system functions operate normally, including the setting of the Line Status and Modem Status registers.

Bit	Function
7 - 4	Reserved = 0
3	Modem-Status Interrupt
2	Receiver-Line-Status Interrupt
1	Transmitter-Holding-Register-Empty Interrupt
0	Received Data Available Interrupt

Figure 4-171. Interrupt Enable Register

Bits 7 - 4 Reserved. These bits are always cleared to 0.

Bit 3 When set to 1, this bit enables the modem-status interrupt.

Bit 2 When set to 1, this bit enables the receiver-line-status interrupt.

Bit 1 When set to 1, this bit enables the transmitter-holding-register-empty interrupt.

Bit 0 When set to 1, this bit enables the received-data-available interrupt.

Interrupt Identification Register (hex nFA)

In order to minimize programming overhead during data character transfers, the controller prioritizes interrupts into four levels:

- Priority 1 - Receiver-line-status
- Priority 2 - Received-data-available
- Priority 3 - Transmitter-holding-register-empty
- Priority 4 - Modem status.

Information about a pending interrupt is stored in the Interrupt Identification register. When the Interrupt Identification register is addressed, the pending interrupt with the highest priority is held and no other interrupts are acknowledged until the system microprocessor services that interrupt.

Bit	Function
7 - 3	Reserved = 0
2	Interrupt ID, Bit 1
1	Interrupt ID, Bit 0
0	Interrupt Pending = 0

Figure 4-172. Interrupt Identification Register

Bits 7 - 3 Reserved. These bits are always cleared to 0.

Bits 2, 1 These two bits identify the pending interrupt with the highest priority, as shown in Figure 4-173 on page 4-162.

Bit 0 When this bit is set to 1, no interrupt is pending, and polling (if used) continues. When this bit is cleared to 0, an interrupt is pending, and the contents of this register can be used as a pointer to the appropriate interrupt service routine.

This bit can be used in either hard-wired, prioritized, or polled conditions to indicate if an interrupt is pending.

Bits 2 - 0 select Interrupt Control Functions as shown in the following figure:

Bits 2 1 0	Priority	Type	Cause	Interrupt Reset Control
0 0 1	-	None	None	-
1 1 0	Highest	Receiver Line Status	Overrun, Parity, or Framing Error or Break Interrupt	Read the Line Status Register
1 0 0	Second	Received Data Available	Data in Receiver Buffer	Read the Receiver Buffer Register
0 1 0	Third	Transmitter Holding Register Empty	Transmitter Holding Register is Empty	Read Interrupt Identification register or Write to Transmitter Holding Register
0 0 0	Fourth	Modem Status	Change in signal status from modem	Read the Modem Status Register

Figure 4-173. Interrupt Control Functions

Line Control Register (hex nFB)

The format of asynchronous communications is programmed through the Line Control register.

Bit	Function
7	Divisor Latch Access Bit
6	Set Break
5	Stick Parity
4	Even Parity Select
3	Parity Enable
2	Number of Stop Bits
1	Word Length Select, Bit 1
0	Word Length Select, Bit 0

Figure 4-174. Line Control Register (LCR)

Bit 7 This bit must be set to 1 during a read or write operation to gain access to the divisor latches of the baud-rate generator. It must be cleared to 0 to gain access to the Receiver Buffer, Transmitter Holding, or Interrupt Enable registers.

Bit 6 When this bit is set to 1 set-break is enabled, serial output is forced to the spacing state and remains there regardless of other transmitter activity. When this bit is cleared to 0, set-break is disabled.

Bit 5 When bits 5, 4, and 3 are set to 1, the parity bit is sent and checked as a logical 0. When bits 5 and 3 are set to 1, and bit 4 is cleared to 0, the parity bit is sent and checked as a logical 1.

Bit 4 When this bit and bit 3 are set to 1, an even number of logical ones are transmitted and checked in the data word bits and parity bit. When this bit is cleared to 0, and bit 3 is set to 1, an odd number of logical ones are transmitted and checked in the data word bits and parity bit.

Bit 3 When set to 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit. (The parity bit is used to produce an even or odd number of ones when the data-word bits and the parity bit are summed.)

Bit 2 This bit, along with bits 0 and 1, specifies the number of stop bits in each serial character that is sent or received as shown in the following figure:

Bit 2	Word Length *	Number of Stop Bits
0	N/A	1
1	5-Bits	1-1/2
1	6-Bits	2
1	7-Bits	2
1	8-Bits	2

* Word Length is specified by bits 1 and 0 in this register.

Figure 4-175. Stop Bits

Bits 1, 0 These two bits specify the number of bits in each serial character that is sent or received. Word length is selected as shown in the following figure:

Bit 1 0	Word Length
0 0	5-Bits
0 1	6-Bits
1 0	7-Bits
1 1	8-Bits

Figure 4-176. Word Length

Modem Control Register (hex nFC)

This 8-bit register controls the data exchange with the modem, data set, or peripheral device emulating a modem.

Bit	Function
7 - 5	Reserved = 0
4	Loop
3	Out 2
2	Out 1
1	Request-to-Send
0	Data-Terminal-Ready

Figure 4-177. Modem Control Register (MCR)

Bits 7 - 5 Reserved. These bits are always cleared to 0.

Bit 4 This bit provides a loopback feature for diagnostic testing of the serial port. When bit 4 is set to 1:

- Transmitter-serial-output is set to the marking state.
- Receiver-serial-input is disconnected.
- Output of the Transmitter Shift register is "looped back" to the Receiver Shift register input.

  Note: The Transmitter and Receiver Shift registers are not accessible NS16550 registers.

- The modem control inputs (CTS, DSR, DCD, and RI) are disconnected.
- The modem control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four modem control inputs.
- The modem control output pins are forced inactive.

When the serial port is in the diagnostic mode, transmitted data is immediately received. This feature allows the system microprocessor to verify the transmit-data and receive-data paths of the serial port.

When the serial port is in the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but their sources are the lower four bits of the Modem Control register instead of the four modem control input signals. The interrupts are still controlled by the Interrupt Enable register.

Bit 3 This bit controls the 'output 2' (OUT 2) signal which is an auxiliary user-designated interrupt enable signal. OUT 2 is used to control the interrupt signal to the channel. Setting this bit to 1 enables the interrupt. Clearing this bit to 0 disables the interrupt.

Bit 2 This bit controls the 'output 1' (OUT 1) signal which is an auxiliary user-designated output signal. When set to 1, OUT 1 is forced active. When cleared to 0, OUT 1 is forced inactive.

Bit 1 This bit controls the 'request-to-send' (RTS) modem control output signal. When set to 1, RTS is forced active. When cleared to 0, RTS is forced inactive.

Bit 0 This bit controls the 'data-terminal-ready' (DTR) modem control output signal. When set to 1, DTR is forced active. When cleared to 0, DTR is forced inactive.

Line Status Register (hex nFD)

This 8-bit register provides the system microprocessor with status information about the data transfer.

Bit	Function
7	Reserved = 0
6	Transmitter Shift Register Empty (TEMT)
5	Transmitter Holding Register Empty (THRE)
4	Break Interrupt (BI)
3	Framing Error (FE)
2	Parity Error (PE)
1	Overrun Error (OR)
0	Data Ready (DR)

Figure 4-178. Line Status Register (LSR)

Bit 7 Reserved. This bit is always cleared to 0.

Bit 6 This bit is set to 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. It is cleared to 0 when either the Transmitter Holding register or the Transmitter Shift register contains a data character.

Bit 5 This bit indicates that the serial port controller is ready to accept a new character for transmission. This bit is set to 1 when a character is transferred from the Transmitter Holding register into the Transmitter Shift register. This bit is cleared to 0 when the system microprocessor loads the Transmitter Holding register.

This bit also causes the controller to issue an interrupt to the system microprocessor when bit 1 in the Interrupt Enable register is set to 1.

Bit 4 This bit is set to 1 when the received data input is held in the spacing state for longer than a fullword transmission time (that is, the total time of start bit + data bits + parity + stop bits).

Note: Bits 1 through 4 are the error conditions that produce a receiver line-status interrupt whenever any of the corresponding conditions are detected.

Bit 3 This bit is set to 1 when the stop bit, following the last data bit or parity bit, is at a spacing level. This indicates that the received character did not have a valid stop bit.

Bit 2 This bit is set to 1 when a parity error is detected (the received character does not have the correct even or odd parity, as selected by the even-parity-select bit). This bit is cleared to 0 when the system microprocessor reads the contents of the Line Status register.

Bit 1 When set to 1, this bit indicates that data in the Receiver Buffer register was not read by the system microprocessor before the next character was transferred into the Receiver Buffer register, destroying the previous character. This bit is cleared to 0 when the system microprocessor reads the contents of the Line Status register.

Bit 0 This bit is set to 1 when a complete incoming character has been received and transferred into the Receiver Buffer register. This bit is cleared to 0 by reading the Receiver Buffer register.

Modem Status Register (hex nFE)

This 8-bit register provides the current state of the control lines from the modem (or external device) to the system microprocessor. In addition, bits 3 through 0 of this register provide change information. These four bits are set to logical 1 whenever a control input from the modem changes state. They are reset to logical 0 whenever the system microprocessor reads this register.

Bit	Function
7	Data-Carrier-Detect
6	Ring Indicator
5	Data-Set-Ready
4	Clear-to-Send
3	Delta-Data-Carrier-Detect
2	Trailing Edge Ring Indicator
1	Delta-Data-Set-Ready
0	Delta-Clear-to-Send

Figure 4-179. Modem Status Register (MSR)

Bit 7 This bit is the inverted ‘data-carrier-detect’ modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 3 in the Modem Control register.

Bit 6 This bit is the inverted 'ring-indicator' modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 2 in the Modem Control register.

Bit 5 This bit is the inverted 'data-set-ready' modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 0 in the Modem Control register.

Bit 4 This bit is the inverted 'clear-to-send' modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 1 in the Modem Control register.

Bit 3 When set to 1, this bit indicates that the 'data-carrier-detect' modem control input signal has changed state since the last time it was read by the system microprocessor.

Note: Whenever bit 0, 1, 2, or 3 is set to 1, a modem status interrupt is generated.

Bit 2 When set to 1, this bit indicates that the 'ring-indicator' modem control input signal has changed from an active condition to an inactive condition.

Bit 1 When set to 1, this bit indicates that the 'data-set-ready' modem control input signal has changed state since the last time it was read by the system microprocessor.

Bit 0 When set to 1, this bit indicates that the 'clear-to-send' modem control input signal has changed state since the last time it was read by the system microprocessor.

Scratch Register

This register does not control the serial port in any way. It can be used by the system microprocessor to temporarily hold data.

Serial Port Controller Programming Considerations

The serial port uses the NS16550 serial communications controller. The NS16550 is functionally compatible with the NS16450 and appears identical to software as the IBM Personal Computer AT serial port on the serial/parallel adapter. See "Hardware Interrupts" on page 9-6 for additional programming considerations.

The serial port can be configured to either Serial 1 or Serial 2 using the system configuration utilities.

Signal Descriptions

Modem Control Input Signals

The following are input signals from the modem or external device to the controller. Bits 7 through 4 in the Modem Status register indicate the condition of these signals. Bits 3 through 0 in the Modem Status register monitor these signals to indicate when the modem changes state.

Clear to Send (CTS): When active, this signal indicates that the modem is ready for the serial port to transmit data.

Data Set Ready (DSR): When active, this signal indicates the modem or data set is ready to establish the communications link and transfer data with the controller.

Ring Indicator (RI): When active, this signal indicates the modem or data set detected a telephone ringing signal.

Data Carrier Detect (DCD): When active, this signal indicates that the modem or data set detected a data carrier.

Modem Control Output Signals

The following are controller output signals. They are all set inactive upon a master reset operation. These signals are controlled by bits 3 through 0 in the Modem Control register.

Data Terminal Ready (DTR): When active, this signal informs the modem or data set that the controller is ready to communicate.

Request to Send (RTS): When active, this signal informs the modem or data set that the controller is ready to send data.

Output 1 (OUT 1): This signal is pulled high.

Output 2 (OUT 2): User-designated output. This signal controls interrupts to the system.

Voltage Interchange Information

The signal is considered in the *marking* condition when the voltage on the interchange circuit, measured at the interface point, is more negative than -3 Vdc with respect to signal ground. The signal is considered in the *spacing* condition when the voltage is more positive than +3 Vdc with respect to signal ground. The region between +3 Vdc and -3 Vdc is defined as the transition region, and considered an invalid level. The voltage that is more negative than -15 Vdc or more positive than +15 Vdc is also considered an invalid level.

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	On
Negative Voltage	Binary 1	Marking	Off

Figure 4-180. Voltage Levels

Connector

The interface uses the standard D-shell connector and pin assignments defined for RS-232-C. The voltage levels are EIA only. Current loop interface is not supported.

The following figure shows the pin assignments for the serial port in a communications environment.

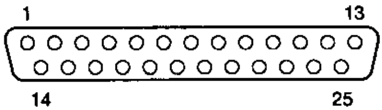

Figure 4-181. Serial Port Connector

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	NA	Not Connected	14	NA	Not Connected
2	O	Transmit Data	15	NA	Not Connected
3	I	Receive Data	16	NA	Not Connected
4	O	Request to Send	17	NA	Not Connected
5	I	Clear to Send	18	NA	Not Connected
6	I	Data Set Ready	19	NA	Not Connected
7	NA	Signal Ground	20	O	Data Terminal Ready
8	I	Data Carrier Detect	21	NA	Not Connected
9	NA	Not Connected	22	I	Ring Indicate
10	NA	Not Connected	23	NA	Not Connected
11	NA	Not Connected	24	NA	Not Connected
12	NA	Not Connected	25	NA	Not Connected
13	NA	Not Connected			

Figure 4-182. Serial Port Connector Signal and Voltage Assignments

Parallel Port Controller

The parallel port allows the attachment of various devices that transfer 8 bits of parallel data at standard TTL levels. It has a 25-pin, D-shell connector. This port may be addressed as parallel port 1, 2, or 3.

The parallel port is designed to be compatible with previous IBM Personal Computer parallel port implementations. The primary function of the parallel port is to attach a printer with a parallel interface to the system. The parallel port has an extended mode that allows support of bidirectional input and output. The port also supports level sensitive interrupts and a readable interrupt pending status.

The following figure is a block diagram of the parallel port controller.

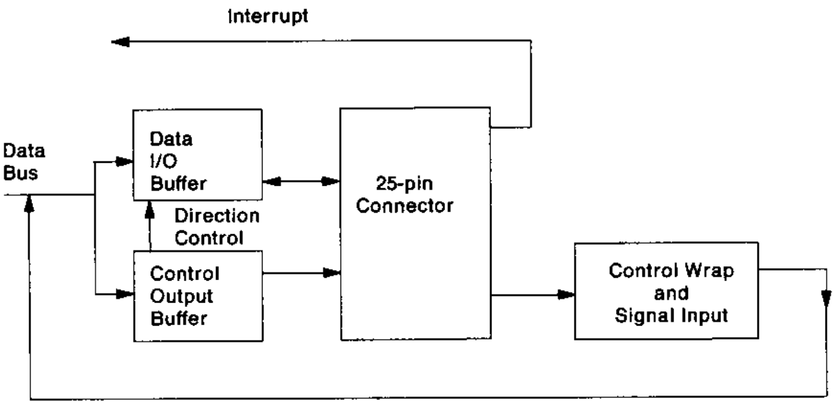

Figure 4-183. Parallel Port Controller Block Diagram

Parallel Port Programmable Option Select

The parallel port can be configured to three different address spaces previously used in IBM Personal Computer products. These addresses are selected by placing the system board in Setup (see "Programmable Option Select" on page 2-21) and performing an I/O write to port hex 0102. Bits 6 and 5 in port hex 0102 are used to select the address spaces shown below.

Bit 6	Bit 5	Function
0	0	Parallel 1
0	1	Parallel 2
1	0	Parallel 3

Figure 4-184. Parallel Port Configuration

The address assignments for each configuration are shown in the following figure.

	Data Address (hex)	Status Address (hex)	Parallel Control Address (hex)
Parallel 1	03BC	03BD	03BE
Parallel 2	0378	0379	037A
Parallel 3	0278	0279	027A

Figure 4-185. Parallel Port Address Assignments

Parallel Port Extended Mode

The extended mode option of the parallel port is selected through Programmable Option Select. With the system board in Setup, the extended mode is selected by writing a 0 to bit 7 of I/O address hex 0102. The extended mode makes the parallel port an 8-bit parallel and bidirectional interface. The following figure shows the possible configurations for the parallel port in the extended mode.

Port Mode	Port Direction	POS Mode Bit	Parallel Control Direction Bit	System Reset
Extended	Write	0	0	1
Extended	Write	0	0	0
Extended	Read	0	1	0
Compatible	Write	1	NA	0

Figure 4-186. Parallel Port Extended Mode Configurations

Parallel Port Controller Programming Considerations

The following are some considerations for programming the parallel port controller.

The interface responds to five I/O instructions: two output and three input. In the compatible mode, the output instructions transfer data into two latches whose outputs are presented on the pins of the D-shell connector. In the extended mode, the 8-bit data latch output to the D-shell connector is controlled by bit 5 in the Parallel Control port.

In the compatible mode, two of the three input instructions allow the processor to read back the contents of the two latches. In the extended mode, the read-back of the 8-bit data in the Data Address is controlled by bit 5 in the Parallel Control port. The third input instruction allows the system microprocessor to read the real-time status of a group of pins on the connector.

The extended mode can be used by externally attached equipment.

During POST the parallel port is configured as an output port. POST status information is written to this port during the power-on initialization as well as initialization after a reset from the keyboard (Ctrl, Alt, Del).

The following is a detailed description of each interface port instruction. For specific signal timing parameters, refer to the specifications for the equipment connected to the parallel port connector.

Data Address Port

The Data Address port is the 8-bit data port for both the compatible and extended modes. For the compatible mode, a write operation to this port immediately presents data to the connector pins. A read operation from this port in the compatible mode produces the data that was last written to it.

In the extended mode, a write operation to this port latches the data but it is only presented to the connector pins if the direction bit was set to Write in the Parallel Control port. A Read operation in the extended mode produces either:

- The data previously written if the direction bit in the Parallel Control port is set to Write.
- The data on the connector pins from another device if the direction bit is set to Read.

Port Bit	Port Data
Bit 7 - 0	Data

Figure 4-187. Data Address Port

Bits 7 - 0 These bits represent the 'data' (D7 - D0) signal lines.

Status Port

The status port is a read-only port in either mode. A read operation to this port presents the system microprocessor with the interrupt pending status of the interface as well as the real-time status of the connector pins as shown in the following figure. An interrupt is pending when the interrupt status bit is set to 0.

Port Bit	Port Data
Bit 7	-BUSY
Bit 6	-ACK
Bit 5	PE
Bit 4	SLCT
Bit 3	-ERROR
Bit 2	-IRQ Status
Bit 1, 0	Reserved

Figure 4-188. Status Port

Bit 7 This bit represents the state of the '-busy' (-BUSY) signal. When this signal is active, the printer is busy and cannot accept data.

Bit 6 This bit represents the current state of the printer '-acknowledge' (-ACK) signal. When this bit is set to 0, the printer has received a character and is ready to accept another.

Bit 5 This bit represents the current state of the printer 'paper end' (PE) signal. When this bit is set to 1, the printer has detected the end of the paper.

Bit 4 This bit represents the current state of the 'select' (SLCT) signal. When this bit is set to 1, the printer has been selected.

Bit 3 This bit represents the current state of the printer '-error' (-ERROR) signal. When this bit is set to 0, the printer has encountered an error condition.

Bit 2 When this bit is set to 0, the printer has acknowledged the previous transfer using the '-acknowledge' signal.

Bits 1, 0 Reserved

Parallel Control Port

The Parallel Control port is a read or write port. A write operation to this port latches the six least-significant data bits of the bus. The sixth bit corresponds to the direction control bit and is only applicable in the extended mode. The remaining five bits are compatible with previous implementations as shown in the following figure. A read operation to the Parallel Control port presents the system microprocessor the data that was last written to it, with the exception of the write-only direction bit.

Port Bit	Port Data
Bit 7, 6	Reserved
Bit 5	Direction
Bit 4	IRQ EN
Bit 3	Pin 17 (SLCT IN)
Bit 2	Pin 16 (-INIT)
Bit 1	Pin 14 (AUTO FD XT)
Bit 0	Pin 1 (STROBE)

Figure 4-189. Parallel Control Port

Bits 7, 6 Reserved

Bit 5 This bit controls the direction of the data port. For more information on the use of this bit see Figure 4-186 on page 4-173. This is a write-only bit.

Bit 4 This bit enables the parallel port interrupt. When this bit is set to 1, an interrupt occurs when the '-acknowledge' signal changes from active to inactive.

Bit 3 This bit controls the 'select in' (SLCT IN) signal. When this bit is set to 1, the printer is selected.

Bit 2 This bit controls the 'initialize printer' (-INIT) signal. When this bit is set to 0, the printer starts.

Bit 1 This bit controls the 'automatic feed XT' (AUTO FD XT) signal. When this bit is set to 1, the printer will automatically line feed after each line is printed.

Bit 0 This bit controls the 'strobe' signal to the printer. When this bit is set to 1, data is pulse-clocked into the printer.

Parallel Port Timing

The timing for the parallel port depends on the timing of the devices connected to the port. The following diagram shows the sequence for typical parallel port signal timing.

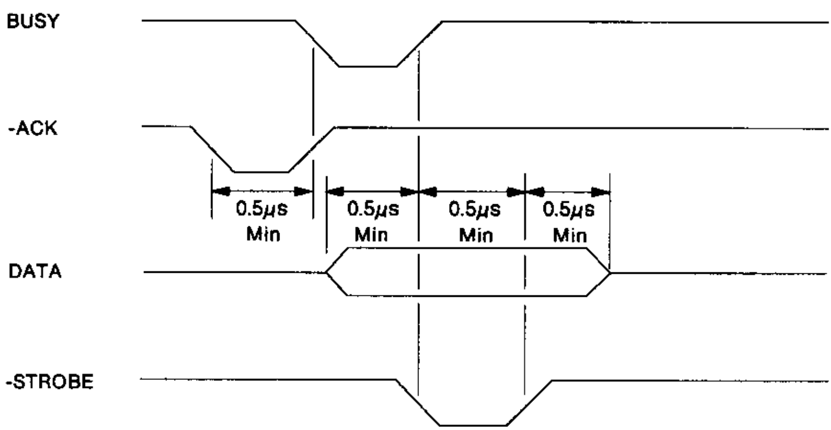

Figure 4-190. Parallel Port Timing Sequence.

Signal Descriptions

The following figures list characteristics of the signals.

Sink Current	24 mA	Maximum
Source Current	15 mA	Maximum
High-level Output Voltage	2.4 Vdc	Minimum
Low-level Output Voltage	0.5 Vdc	Maximum

Figure 4-191. Data and Interrupt Signals

Pins 1, 14, 16, and 17 are driven by open collector drivers pulled to 5 Vdc through 4.7 kilohm resistors.

Sink Current	20 mA	Maximum
Source Current	0.55 mA	Maximum
High-level Output Voltage	5.0 Vdc minus pullup	Minimum
Low-level Output Voltage	0.5 Vdc	Maximum

Figure 4-192. Control Signals

Connector

The parallel port connector is a standard 25-pin D-shell connector. The D0 - D7 lines on the connector are driven by drivers capable of sourcing 15 milliamps and sinking 24 milliamps.

The following are the voltages and signals assigned to the parallel port controller connector.

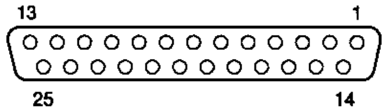

Figure 4-193. Parallel Port Connector

Pin No.	I/O	Signal Name	Pin No.	I/O	Signal Name
1	I/O	-STROBE	14	O	-AUTO FEED XT
2	I/O	Data Bit 0	15	I	-ERROR
3	I/O	Data Bit 1	16	O	-INIT
4	I/O	Data Bit 2	17	O	-SLCT IN
5	I/O	Data Bit 3	18	NA	Ground
6	I/O	Data Bit 4	19	NA	Ground
7	I/O	Data Bit 5	20	NA	Ground
8	I/O	Data Bit 6	21	NA	Ground
9	I/O	Data Bit 7	22	NA	Ground
10	I	-ACK	23	NA	Ground
11	I	BUSY	24	NA	Ground
12	I	PE	25	NA	Ground
13	I	SLCT			

Figure 4-194. Parallel Port Connector Signal and Voltage Assignments

Memory

The system has the following types of memory:

- Read Only Memory (ROM)
- Random Access Memory (RAM)
- Real-Time Clock/Complementary Metal Oxide Semiconductor RAM (RT/CMOS RAM).

Read Only Memory (ROM) Subsystem

The system board ROM subsystem consists of four 32K by 8-bit modules in a 64K by 16-bit arrangement. ROM is assigned at the top of the first and last 1M address space (hex 0E0000 and FE0000). ROM is not parity-checked.

Random Access Memory (RAM) Subsystem

The system board RAM subsystem starts at address hex 000000 of the 16M address space. It consists of 1M of RAM modules. The Model 50 uses two, 512K by 9 memory module packages and the Model 60 uses four, 256K by 9 memory module packages. The RAM operates with one wait state. Memory-refresh requests occur once every 15 microseconds.

Note: The memory must be accessed or refreshed 512 times before it can be used.

The timing of the memory signals is similar to the timings for the Hitachi HB61009BR-15 256K-by-9 150 nanosecond DRAM or equivalent.

Each memory module package connects to a 30-pin connector, The pins are numbered sequentially. On the Model 50 system board pin 1 is the pin closest to the front of the system unit. On the Model 60 system board pin 1 is closest to the top of the system unit.

The following shows the pin definitions for the memory module package sockets.

Pin	I/O	Signal	Pin	I/O	Signal
1	N/A	5 Vdc	2	I	-Column Address Strobe
3	I/O	Data Bit 1	4	I	Address Bit 1
5	I	Address Bit 2	6	I/O	Data Bit 2
7	I	Address Bit 3	8	I	Address Bit 4
9	N/A	Ground	10	I/O	Data Bit 3
11	I	Address Bit 5	12	I	Address Bit 6
13	I/O	Data Bit 4	14	I	Address Bit 7
15	I	Address Bit 8	16	I/O	Data Bit 5
17	I	Address Bit 9	18	N/A	No Connection
19	I	RAS 1 *	20	I/O	Data Bit 6
21	I	-Write Strobe	22	N/A	Ground
23	I/O	Data Bit 7	24	O	Presence Detect 1
25	I/O	Data Bit 8	26	O	Presence Detect 2
27	I	Row Address Strobe	28	N/A	No Connection
29	I/O	Data Bit 9 (Parity)	30	N/A	+5 Vdc

* 512K memory module packages only.

Figure 4-195. System Board Memory Module Package Connector Pin Assignments

The following shows the mapping for the memory locations on the Model 50 and Model 60 system boards.

Hex Range	Function
000000 to 09FFFF	640K System Board RAM *
0A0000 to 0BFFFF	128K Video RAM
0C0000 to 0DFFFF	128K I/O Expansion ROM
0E0000 to 0FFFFF	128K System Board ROM
100000 to 15FFFF	384K System Board RAM
160000 to FDFFFF	Channel Expansion Memory Addresses
FE0000 to FFFFFF	128K System Board ROM

* A 256-byte portion of this RAM is reserved as a BIOS data area. A 1K portion of this RAM is reserved as an extended BIOS data area. See the IBM Personal System/2 and Personal Computer BIOS Interface Technical Reference for details.

Figure 4-196. System Board Memory Map

Note: With the system board in setup (see "System Board Setup" on page 2-24) the system board memory can be disabled by a command to bit 0 of Port hex 0103. When set to 1, bit 0 enables the memory. When set to 0, this bit disables the memory. The entire 1M of storage is enabled or disabled by this operation.

Real-Time Clock/Complementary Metal Oxide Semiconductor RAM

The real-time clock/complementary metal oxide semiconductor (RT/CMOS) RAM chip (Motorola MC146818A) contains the real-time clock and 64 bytes of nonvolatile RAM. The internal clock circuitry uses 14 bytes of this memory, and the rest is allocated to configuration and system status information.

The Model 60 has in addition to the 64 bytes of nonvolatile RAM, a 2K nonvolatile RAM extension that contains configuration information and other system information.

A 6 Vdc lithium battery maintains voltage to the RT/CMOS when the power supply is not in operation. In addition, the Model 60 uses this battery to maintain the voltage to the 2K CMOS RAM extension.

The system unit cover for both systems can be physically locked to prevent unauthorized access to the battery. This helps prevent unauthorized battery removal and loss of password and configuration information.

The following figure shows the RT/CMOS RAM bytes and their addresses.

Address (hex)	Function
000 - 00D	Real-Time Clock Information
00E	Diagnostic Status Byte
00F	Shut Down Status Byte
010	Diskette Drive Byte
011	First Fixed Disk Type Byte
012	Second Fixed Disk Type Byte
013	Reserved
014	Equipment Byte
015 - 016	Low and High Base Memory Bytes
017 - 018	Low and High Memory Expansion Bytes
019 - 031	Reserved
032 - 033	Configuration CRC Bytes
034 - 036	Reserved
037	Date Century Byte
038 - 03F	Reserved

Figure 4-197. RT/CMOS RAM Address Map

RT/CMOS RAM I/O Operations

When performing I/O operations to the RT/CMOS RAM addresses (described in Figure 4-197 and the following pages), interrupts should be inhibited to avoid having interrupt routines change the CMOS address register before data is read or written. Port hex 0070 should be left to point to Status register D of the RT/CMOS.

The following steps are required to perform I/O operations to the RT/CMOS RAM addresses:

1. OUT to port hex 0070 with the RT/CMOS address that will be written to.

   Note: The NMI mask bit resides in port hex 0070 (see "Nonmaskable Interrupt" on page 3-22).

2. OUT to port hex 0071 with the data to be written.

Reading RT/CMOS RAM requires the following steps:

1. OUT to port hex 0070 with the CMOS address that is to be read from.
2. IN from port hex 0071, and the data read is returned in the AL register.

Warning: When writing port hex 0070, a read to port hex 0071 must be accessed immediately. Failure to do this may cause intermittent malfunctions and unreliable operation of the MC146818A Real-Time Clock/Complementary Metal Oxide Semiconductor RAM.

Real-Time Clock

The following shows bit definitions for the real-time clock bytes (addresses hex 000 - 00D).

Address (hex)	Function	Byte Number
000	Seconds	0
001	Second Alarm	1
002	Minutes	2
003	Minute Alarm	3
004	Hours	4
005	Hour Alarm	5
006	Day Of Week	6
007	Date Of Month	7
008	Month	8
009	Year	9
00A	Status Register A	10
00B	Status Register B	11
00C	Status Register C	12
00D	Status Register D	13

Figure 4-198. Real-Time Clock (Addresses Hex 000 - 00D)

Note: The Setup program initializes registers A, B, C, and D when the time and date are set. Also, Interrupt hex 1A is the BIOS interface to read and set the time and date. It initializes the status bytes the same as the Setup program.

Status Register A

Bit 7 Update in Progress (UIP)—When set to 1, this bit indicates the time update cycle is in progress. When set to 0, this bit indicates the current date and time is available to read.

Bits 6 - 4 22-Stage Divider (DV2 through DV0)—These three divider-selection bits identify which time-base frequency is being used. The system initializes the stage divider to 010, which selects a 32.768 kHz time base. This is the only stage divider supported by the system unit for proper time keeping.

Bits 3 - 0 Rate Selection Bits (RS3 through RS0)—These bits allow the selection of a divider output frequency. The system initializes the rate selection bits to 0110, which selects a 1.024 kHz square-wave output frequency and a 976.562 microsecond periodic interrupt rate.

Status Register B

Bit 7	Set—When set to 0, this bit updates the cycle normally by advancing the counts at one per second. When set to 1, this bit aborts any update cycle in progress and the program can initialize the 14 time-bytes without any further updates occurring until a 0 is written to this bit.
Bit 6	Periodic Interrupt Enable (PIE)—This bit is a read/write bit that allows an interrupt to occur at a rate specified by the rate and divider bits in register A. When set to 1, this bit enables an interrupt. When set to 0, the interrupt is disabled. The system initializes this bit to 0.
Bit 5	Alarm Interrupt Enable (AIE)—When set to 1, this bit enables the alarm interrupt. When set to 0, the alarm interrupt is disabled. The system initializes this bit to 0.
Bit 4	Update-Ended Interrupt Enabled (UIE)—When set to 1, this bit enables the update-ended interrupt. When set to 0 the update-ended interrupt is disabled. The system initializes this bit to 0.
Bit 3	Square Wave Enabled (SQWE)—When set to 1, this bit enables the square-wave frequency as set by the rate selection bits in register A. When set to 0, square wave is disabled. The system initializes this bit to 0.
Bit 2	Date Mode (DM)—This bit indicates whether the time and date calendar updates are to use binary or binary-coded-decimal (BCD) formats. When set to 1, this bit indicates a binary format. When set to 0, a BCD format is indicated. The system initializes this bit to 0.
Bit 1	24/12—This bit establishes whether the hours byte is in the 24-hour or 12-hour mode. When set to 1, this bit indicates the 24-hour mode. When set to 0, the 12-hour mode is indicated. The system initializes this bit to 1.
Bit 0	Daylight Savings Enabled (DSE)—When set to 1, this bit enables daylight savings time. When set to 0, this bit disables daylight savings time (reverts to standard time). The system initializes this bit to 0.

Status Register C

Bits 7 - 4 IRQF, PF, AF, UF—These flag bits are read-only and are affected when the AIE, PIE, and UIE interrupts are enabled with register B.

Bits 3 - 0 Reserved

Status Register D

Bit 7 Valid RAM Bit (VRB)—This bit is read-only and indicates the condition of the contents of the CMOS RAM through the power sense pin. A low state of the power sense pin indicates the real-time clock has lost its power (battery dead). When set to 1, this bit indicates power on the real-time clock. When set to 0, this bit indicates that the real-time clock has lost power.

Bits 6 - 0 Reserved

CMOS RAM Configuration

The following shows the bit definitions for the CMOS configuration bytes (addresses hex 00E - 03F).

Diagnostic Status Byte (Hex 00E)

Bit 7 Indicates the real-time clock chip has lost power. When set to 0, this bit indicates the chip has not lost power. When set to 1, this bit indicates the chip has lost power.

Bit 6 Configuration record and checksum status—When set to 0, this bit indicates the checksum is correct. When set to 1, the checksum is incorrect.

Bit 5 Incorrect configuration—This is a check, at power-on time, of the equipment byte of the configuration record. When set to 0, this bit indicates that the configuration information is correct. When set to 1, the configuration information is incorrect. Power-on checks require at least one diskette drive installed (bit 0 of the equipment byte set to 1).

Bit 4 Memory Size Miscompare—When set to 0, this bit indicates the power-on check determined the same memory size as in the configuration record. When set to 1, the memory size is different.

Bit 3 Fixed Disk Controller/Drive C Initialization Status—When set to 0, this bit indicates the controller and fixed disk drive C are functioning properly and the system can attempt a power-on reset. When set to 1, the controller and/or drive C failed initialization, which prevents the system from attempting a power-on-reset.

Bit 2 Time Status Indicator (POST validity check)—When set to 0, this bit indicates the time is valid. When set to 1, the time is invalid.

Bit 1 This bit indicates whether or not the installed adapters match the configuration information. When set to 0, this bit indicates the adapters match the configuration. When set to 1, the adapters do not match the configuration.

Bit 0 When set to 1, this bit indicates a time-out occurred while trying to read an adapter ID. When set to 0, no timeout occurred.

Shut Down Status Byte (Hex 00F): The bits in this byte are defined by the power-on diagnostics.

Diskette Drive Type Byte (Hex 010)

Bits 7 - 4 Type of first diskette drive:

- **0000** No drive present
- **0001** Double-sided diskette drive (48 tracks per inch, 360K)
- **0010** Reserved
- **0011** High-capacity diskette drive (720K)
- **0100** High-density diskette drive (1.44M)

Note: 0101 through 1111 are reserved.

Bits 3 - 0 Type of second diskette drive installed:

- **0000** No drive present

0001 Double-sided diskette drive (48 tracks per inch, 360K)

0010 Reserved

0011 High-capacity diskette drive (720K)

0100 High-density diskette drive (1.44M)

Note: 0101 through 1111 are reserved.

First Fixed Disk Type Byte (Hex 011): Bits 7 through 0 define the type of first fixed disk drive (drive C) installed. Hex 00 indicates a fixed disk drive is *not* present. See Figure 4-199 on page 4-190 for specific fixed disk drive types.

Second Fixed Disk Type Byte (Hex 012): Bits 7 through 0 define the type of second fixed disk drive (drive D) installed. Hex 00 indicates a fixed disk drive is *not* present. See Figure 4-199 on page 4-190 for specific fixed disk drive types.

The following figure shows the BIOS fixed disk parameters.

Type	Number of Cylinders	Number of Heads	Number Write Precompensation	Landing Zone	Defect Map
0 (0H)		—No fixed disk installed—			No
1 (1H)	306	4	128	305	No
2 (2H)	615	4	300	615	No
3 (3H)	615	6	300	615	No
4 (4H)	940	8	512	940	No
5 (5H)	940	6	512	940	No
6 (6H)	615	4	0FFFFH (none)	615	No
7 (7H)	462	8	256	511	No
8 (8H)	733	5	0FFFFH (none)	733	No
9 (9H)	900	15	0FFFFH (none)	901	No
10 (AH)	820	3	0FFFFH (none)	820	No
11 (BH)	855	5	0FFFFH (none)	855	No
12 (CH)	855	7	0FFFFH (none)	855	No
13 (DH)	306	8	128	319	No
14 (EH)	733	7	0FFFFH (none)	733	No
15 (FH)			—Reserved—		
16 (10H)	612	4	0 (all cyl.)	663	No
17 (11H)	977	5	300	977	No
18 (12H)	977	7	0FFFFH (none)	977	No
19 (13H)	1024	7	512	1023	No
20 (14H)	733	5	300	732	No
21 (15H)	733	7	300	732	No
22 (16H)	733	5	300	733	No
23 (17H)	306	4	0 (all cyl.)	336	No
24 (18H)	612	4	305	663	No
25 (19H)	306	4	0FFFFH (none)	340	No
26 (1AH)	612	4	0FFFFH (none)	670	No
27 (1BH)	698	7	300	732	Yes
28 (1CH)	976	5	488	977	Yes
29 (1DH)	306	4	0 (all cyl.)	340	No
30 (1EH)	611	4	306	663	Yes
31 (1FH)	732	7	300	732	Yes
32 (20H)	1023	5	FFFFH(none)	1023	Yes

Types 33 (21H) through 255 (FF) are reserved.

Figure 4-199. Fixed Disk BIOS Parameters

Reserved (Hex 013)

Equipment Byte (Hex 014)

Bits 7, 6 Indicates the number of diskette drives installed:

00 One drive

01 Two drives

10 Reserved

11 Reserved

Bits 5, 4 Primary display

- **00** Reserved
- **01** Primary display is attached to the Video Graphics Array in the 40-column mode.
- **10** Primary display is attached to the Video Graphics Array in the 80-column mode.
- **11** Primary display is attached to the Video Graphics Array in monochrome mode.

Bits 3, 2 Reserved.

Bit 1 Math coprocessor bit:

- **0** Math coprocessor not installed.
- **1** Math coprocessor installed.

Bit 0 Diskette drive bit:

- **0** No diskette drives installed.
- **1** Diskette drives installed.

Note: The equipment byte defines basic equipment in the system for power-on diagnostic tests.

Low and High Base Memory Bytes (Hex 015 and 016): These bytes define the amount of memory installed below the 640K address space.

The hex value from these bytes represent the number of 1K-byte blocks of base memory. For example, hex 0280 is equal to 640K. Hex 015 is the low-byte of the base memory size. Hex 016 is the high-byte of the base memory size.

Low and High Memory Expansion Bytes (Hex 017 and 018): These bytes define the amount of memory installed above the 1M address space.

The hex value from these bytes represent the number of 1K byte blocks of expansion memory. For example, hex 0800 is equal to 2048K. Hex 017 is the low-byte of the expansion memory size. Hex 018 is the high-byte of the expansion memory size.

Reserved (Hex 019 through 031)

Configuration CRC Bytes (Hex 032 and 033): These bytes contain the cyclic-redundancy-check data for bytes hex 010 through hex 031 of the 64-byte CMOS. Hex 032 is the high-byte of the configuration CRC. Hex 033 is the low-byte of the configuration CRC.

Reserved (Hex 034 through 036)

Date Century Byte (Hex 037): Bits 7 through 0 of this byte contain the BCD value for the century (BIOS interface to read and set).

Reserved (Hex 038 through 03F)

2K CMOS RAM Extension

The Model 60 system board has a 2K CMOS RAM extension for configuration and diagnostic information. These bytes are reserved.

Miscellaneous System Ports

Ports hex 0061, 0070, and 0092 contain information that is used for system control.

System Control Port B (Hex 0061)

Port B is accessed by I/O read or write operations to I/O address hex 0061. The following shows the bit definitions.

Bit	Function
7	Reset timer 0 output latch (IRQ 0)
6 - 4	Reserved
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 4-200. System Control Port B, Write Operations

Bit	Function
7	Parity Check
6	Channel Check
5	Timer 2 output
4	Toggles with each refresh request
3	Enable Channel Check
2	Enable Parity Check
1	Speaker Data Enable
0	Timer 2 Gate to Speaker

Figure 4-201. System Control Port B, Read Operations

Bit 7 A write operation with this bit set to 1, resets IRQ 0.

For a read operation this bit indicates the state of the Parity Check latch. If the bit is equal to 1, a parity check has occurred.

Bit 6 For a read operation this bit returns the state of the Channel Check latch. If the bit is equal to 1, a Channel Check has occurred.

Bit 5 For a read operation this bit returns the condition of timer/counter 2 'output' signal.

Bit 4 For a read operation this bit toggles for each refresh request.

Bit 3 A write operation with this bit set to 0 enables Channel Check. This bit is set to 1 during a power-on reset. A read operation returns the result of the last write operation to this bit.

Bit 2 A write operation with this bit set to 0 enables Parity Check. This bit is set to 1 during a power-on reset. A read operation returns the result of the last write operation to this bit.

Bit 1 A write operation with this bit set to 1 enables speaker data. This bit is set to 0 during a power-on reset. A read operation returns the result of the last write operation to this bit.

Bit 0 A write operation with this bit set to 1 enables the 'timer 2' gate. Setting this bit to 0 turns the gate off. A read operation returns the result of the last write operation to this bit.

RT/CMOS and NMI Mask (Hex 0070)

Bit	Function
7	Non-maskable Interrupt (NMI)
6	Reserved
5 - 0	RT/CMOS RAM

Figure 4-202. RT/CMOS and NMI Mask

Bit 7 When set to 1, this bit enables the NMI. When set to 0 the NMI is masked off. This bit is cleared to 0 by a power-on reset. This bit is write-only. See "Interrupts" on page 3-22 for more information about the NMI.

Bit 6 Reserved

Bits 5 - 0 See "RT/CMOS RAM I/O Operations" on page 4-183.

Note: Port hex 0071 is used with port hex 0070 to read and write to the RT/CMOS RAM and the NMI Mask register.

System Control Port A (Hex 0092)

Port hex 0092 supports the fixed disk drive light, alternate system microprocessor reset, PASS A20, watchdog timer status, and CMOS security lock. The following shows the bit definitions for port hex 0092.

Bit	Function
7	Fixed Disk activity light bit A
6	Fixed Disk activity light bit B
5	Reserved = 0
4	Watchdog Timer Status
3	Security Lock Latch
2	Reserved = 0
1	Alternate Gate A20
0	Alternate Hot Reset

Figure 4-203. System Control Port A

Bits 7, 6 These read/write bits control the fixed disk activity light. Setting either bit to 1 turns the fixed disk activity light on. Setting both bits to 0 turns the light off. The power-on reset condition of each bit is 0.

Bit 5 Reserved

Bit 4 This read-only bit indicates the watchdog timer status. When this bit is equal to 1 a watchdog timeout has occurred. A 0 means that no watchdog timeout has occurred.

Bit 3 This read/write bit provides the security lock for the secured area of the RT/CMOS. Setting this bit to 1 electrically locks the 8-byte password. Once this bit is set by POST it can only be cleared by turning the system power off and then turning the power on.

Bit 2 Reserved

Bit 1 This read/write bit can be used to control address bit A20 when the microprocessor is in Real Address Mode. When this bit is set to 1, the 'A20' signal is active. When this bit is set to 0, A20 is inactive. This bit is set to 0 during a system reset.

Bit 0 This read/write bit provides an alternate system microprocessor reset function. This function provides an alternate means to reset the system microprocessor to effect a mode switch from the Protected Virtual Address Mode to the Real Address Mode. This mechanism supports operating systems requiring faster operation than is provided by the original implementation on the IBM Personal Computer AT using the Intel 8042. It is provided in addition to the 8042 implementation so that compatibility with existing systems and software is not affected. The alternate system microprocessor reset takes 13.4 microseconds.

This bit must be set to 0 either by a system reset or a write operation. When a write operation changes this bit from 0 to 1, the alternate reset pin is pulsed high for 100 to 125 nanoseconds. The reset occurs after a minimum delay of 6.72 microseconds. After writing this bit from 0 to 1, the latch remains set so POST can read this bit. If the bit is a 0, POST assumes the system was just powered on. If the bit is a 1, POST assumes a switch from the Protected Mode to the Real Mode has taken place.